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## Report Title

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# Electrical performance of monolayer MoS<sub>2</sub> field-effect transistors prepared by chemical vapor deposition

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Molybdenum disulfide (MoS<sub>2</sub>) field effect transistors (FET) were fabricated on atomically smooth large-area single layers grown by chemical vapor deposition. The layer qualities and physical properties were characterized using high-resolution Raman and photoluminescence spectroscopy, scanning electron microscopy, and atomic force microscopy. Electronic performance of the FET devices was measured using field effect mobility measurements as a function of temperature. The back-gated devices had mobilities of 6.0 cm<sup>2</sup>/V s at 300 K without a high- $\kappa$  dielectric overcoat and increased to 16.1 cm<sup>2</sup>/V s with a high- $\kappa$  dielectric overcoat. In addition the devices show on/off ratios ranging from 10<sup>5</sup> to 10<sup>9</sup>. © 2013 AIP Publishing LLC. [<http://dx.doi.org/10.1063/1.4804546>]

Over the past year, two-dimensional metal dichalcogenides have emerged as promising semiconductor materials to complement graphene-based electronics. Like graphene, these materials have highly tunable properties based upon both layer count and the choice of substrate/top gate materials.<sup>1–4</sup> In particular, MoS<sub>2</sub>, which as a bulk material exhibits an indirect bandgap of 1.29 eV and modest electron mobilities, has a direct bandgap of 1.8 eV for a single molecular layer as well as reported field-effect mobilities as high as 470 cm<sup>2</sup>/V s when combined with appropriate substrates and/or overcoats.<sup>5,6</sup> While the latter figure does not compare with the values that can easily be obtained in graphene, MoS<sub>2</sub>, with its large layer number-dependent bandgap, allows for the fabrication of transistors with on/off ratios exceeding 10<sup>7</sup>.<sup>5</sup> Furthermore, MoS<sub>2</sub> also shows promise for use in logic circuits and optoelectronic devices, and it is a promising material for use on flexible and transparent substrates.<sup>7,8</sup>

The vast majority of recent reports on MoS<sub>2</sub>, like the early literature on graphene, are based on samples prepared by mechanical exfoliation.<sup>2</sup> While there have been several reports on monolayer MoS<sub>2</sub> devices, many of these studies utilize few-layer (2–5) MoS<sub>2</sub>, since its exfoliation typically results in flakes with significantly greater thickness and smaller size than what can be readily obtained for graphene.<sup>9,10</sup> In order to fabricate and measure reliable devices properties, large area CVD grown MoS<sub>2</sub> material with controlled layer count and large grain size is required. Recently, several researchers have reported direct growth of MoS<sub>2</sub> films on SiO<sub>2</sub> surfaces using sulfur powder and a thin molybdenum or molybdenum oxide seed layer or remote solid source, and more recent reports have demonstrated complete coverage of areas as large as several square centimeters.<sup>11–14</sup> In the current work we utilized CVD-grown single-layer films with incomplete coverage to fabricate MoS<sub>2</sub> FET devices and measured their electronics properties as a function of temperature as well as investigate the effect of adding a

top atomic layer deposition (ALD) dielectric on device mobility.

Monolayer MoS<sub>2</sub> films confirmed by cross-sectional transmission electron microscopy (X-TEM) were grown directly on a 285 nm SiO<sub>2</sub>/Si substrate using the procedure described in detail by Najmaei *et al.*<sup>13</sup> In brief, high aspect ratio MoO<sub>3</sub> nanoribbons grown using a hydrothermal process were dispersed onto an auxiliary silicon substrate and placed inside a tube furnace with the growth substrates surrounding it. Sulfur powder, placed upstream near the opening of the furnace at an approximate temperature of 600 °C, was sublimated for use as the sulfur vapor source. The furnace was heated to a peak temperature of 850 °C under a constant flow of nitrogen and was held at this set point for 10–15 min and then cooled to room temperature. This process resulted in incomplete growths of 13 ± 2.5 μm single crystal triangles. Electron-beam lithography (EBL) was used to fabricate variable channel length FETs and hall bar structures directly onto single layer material avoiding grain boundaries and other defects. A methyl methacrylate (MMA) and polymethyl methacrylate (PMMA) bilayer resist process was used for all steps. The MoS<sub>2</sub> layer was patterned using a low-power inductively coupled plasma reactive ion etch (ICP-RIE) in a CH<sub>4</sub>/O<sub>2</sub> plasma, and source and drain contacts were deposited using e-beam evaporated Ti/Au (15/85 nm). In order to analyze any damage or variation in the MoS<sub>2</sub> structural chemistry during processing, high-resolution Raman and photoluminescence (PL) imaging was performed on the active device area after each processing step. These measurements were performed with a WITec Alpha 300RA system using the 532 nm line of a frequency-doubled Nd:YAG laser as the excitation source. The spectra were measured in the backscattering configuration using a 100× objective and either a 600 or 1800 grooves/mm grating. The spot size of the laser was ~342 nm resulting in an incident laser power density ~140 μW/μm<sup>2</sup>. No time dependent shifting of the E<sub>2g</sub> and A<sub>1g</sub> modes was produced during testing. Atomic force microscopy (AFM) and field emission scanning electron microscopy (FE-SEM) images were taken on pristine flakes that were not used for

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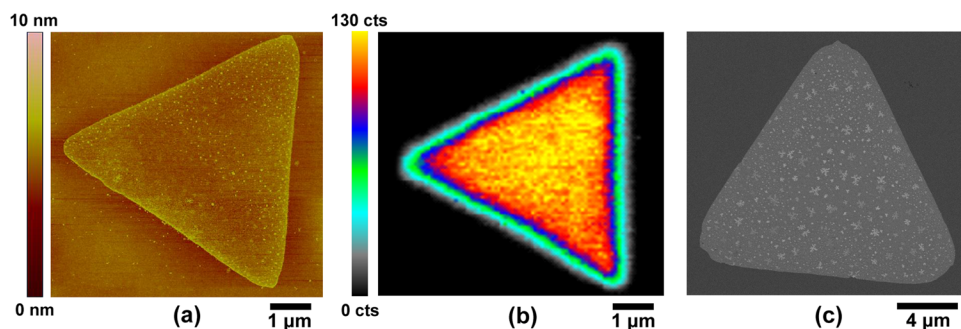


FIG. 1. AFM image (a), high resolution Raman map of the out plane mode intensity (b), and a backscatter FE-SEM image (c) of a typical MoS<sub>2</sub> crystal.

device fabrication<sup>15</sup> to characterize the change in morphology of the films as a result of processing, which will be the focus of an independent, future study. All electrical measurements were obtained with a Keithley 4200 parameter analyzer by using the substrate as a universal back gate from 150 K to 350 K at a pressure of  $2 \times 10^{-6}$  Torr.<sup>16</sup> After initial testing, a 15 nm Al<sub>2</sub>O<sub>3</sub> layer was grown over the samples using ALD performed at 170 °C, and the electrical properties of the devices were re-measured showing the mobility enhancement due to the reduction in Coulomb scattering caused by the high- $\kappa$  dielectric.<sup>5,6</sup>

AFM and Raman images of a typical monolayer crystal are shown in Figures 1(a) and 1(b). This data provides a strong indication that the MoS<sub>2</sub> films are monolayer with a typical thickness of 0.9 nm and a separation of the in- and out-of-plane modes of  $26 \text{ cm}^{-1}$ . While the film thickness we measured by AFM is greater than the 0.6-0.7 nm value which is typically quoted for exfoliated monolayer films, this value is not sufficiently large to suggest bilayer material (1.3 nm thick).<sup>5</sup> Because the growth is performed directly on Si/SiO<sub>2</sub> substrates, the thickness discrepancy is likely a result of interfacial contamination. In addition, PL measurements were taken on the MoS<sub>2</sub> films (not shown) and were found to provide significant edge-enhanced PL similar to CVD tungsten disulfide (WS<sub>2</sub>) films.<sup>17,18</sup> A strong quenching of the PL intensity in bilayer regions, which would be expected due to the direct to indirect bandgap transition, was also observed.<sup>1</sup> Backscatter electron images of an additional crystal are shown in Figure 1(c); the presence of a secondary, dendritic-like growth as well as sub-10 nm triangles with no apparent preferred orientation can be observed from these images. These have not yet been identified as residual MoO<sub>3</sub> or bilayer growth regions on the crystal but are the likely reason for the high AFM step height measurement.

Several devices with varying length (L) and width (W) ratios were fabricated. The  $I_D$ - $V_{GS}$  and  $I_D$ - $V_{DS}$  characteristics of a MoS<sub>2</sub> transistor with an L/W of 400/1000 nm are shown in Figure 2 as a function of temperature at a 1 V drain bias before and after the deposition of an Al<sub>2</sub>O<sub>3</sub> overcoat. It is important to note that the typical contact resistance, which was extracted using the transmission line method for these devices was  $\sim 8 \Omega \text{ mm}$  at 300 K. This is an extremely high value and thus has a significant negative impact on the ultimate performance of these FETs. Recent work has shown that using low work function metals such as Scandium (Sc) in place of Ti/Au can significantly reduce the contact resistance to much more reasonable values on the order of 0.5-1  $\Omega \text{ mm}$ .<sup>19</sup> In fact, this study claims that despite the linear I-V curves produced in few-layer MoS<sub>2</sub>, there still remains a

significant Schottky barrier height at the metal-semiconductor junction at low  $V_{DS}$  when utilizing titanium as the source and drain contacts.<sup>19</sup> This is likely a greater issue in single layer CVD material since the contamination at the interface as well as the large bandgap relative to bi- and few-layer material will tend to increase the barrier height.

The field-effect mobility for these devices was extracted using the following equation:

$$\mu = \frac{dI_{DS}}{dV_{BG}} \cdot \frac{L}{WC_g V_{DS}}, \quad (1)$$

where  $C_g$  is the gate capacitance per unit area, L is the channel length, W is the channel width,  $V_{DS}$  is the source-drain voltage, and  $\frac{dI_{DS}}{dV_{BG}}$  is the slope of the  $I_{DS}$ - $V_{GS}$  characteristics taken in the linear region. All mobility values were calculated at a  $V_{DS}$  of 0.5 V, and the mobility as a function of temperature is shown in Figure 3. At room temperature without a high- $\kappa$  top dielectric we were able to measure a field effect mobility of  $6.0 \text{ cm}^2/\text{Vs}$ , which is very comparable to previously reported values which typically fall within the  $0.5$ - $8.0 \text{ cm}^2/\text{Vs}$  range. Both before and after deposition of the Al<sub>2</sub>O<sub>3</sub> layer, the devices show increasing in mobility with increasing temperature. In studies on few-layer MoS<sub>2</sub>, the mobility has been found to increase with decreasing temperature from 300 K to  $\sim 30$  K which has been attributed to the enhanced scattering of electrons by optical phonons at high temperatures.<sup>20,21</sup> At temperatures below 30 K in few layer exfoliated materials, the decreasing mobility with decreasing temperature has been described by suggesting the presence of trap states, which act as an impurity band.<sup>20</sup> However, mixed results showing both increasing and decreasing mobility with temperature have been published in the literature for single-layer, back-gated MoS<sub>2</sub> FETs prepared with exfoliated material.<sup>21</sup>

Initial studies, as a result of improper dual gating, heavily overestimated the effect of adding top high- $\kappa$  ALD dielectrics (such as HfO<sub>2</sub> and Al<sub>2</sub>O<sub>3</sub> to MoS<sub>2</sub>) to provide more than a 100 times increase in the field effect mobility.<sup>22</sup> For this work, in back-gated devices the Al<sub>2</sub>O<sub>3</sub> layer was found to increase the field-effect mobility by an average of  $3.2 \pm 0.4$  times at 300 K for all of the devices measured in this study. This value is very similar to the degree of improvement in mobility values reported for few layer (10 nm thick) exfoliated materials with low resistance Sc contacts and suggests that the addition of the top dielectric does in fact reduce scattering on the MoS<sub>2</sub> surface and is not a bulk effect. In addition, it provides evidence to rule out reduction in contact resistance as a result of the high- $\kappa$  dielectric resulting in

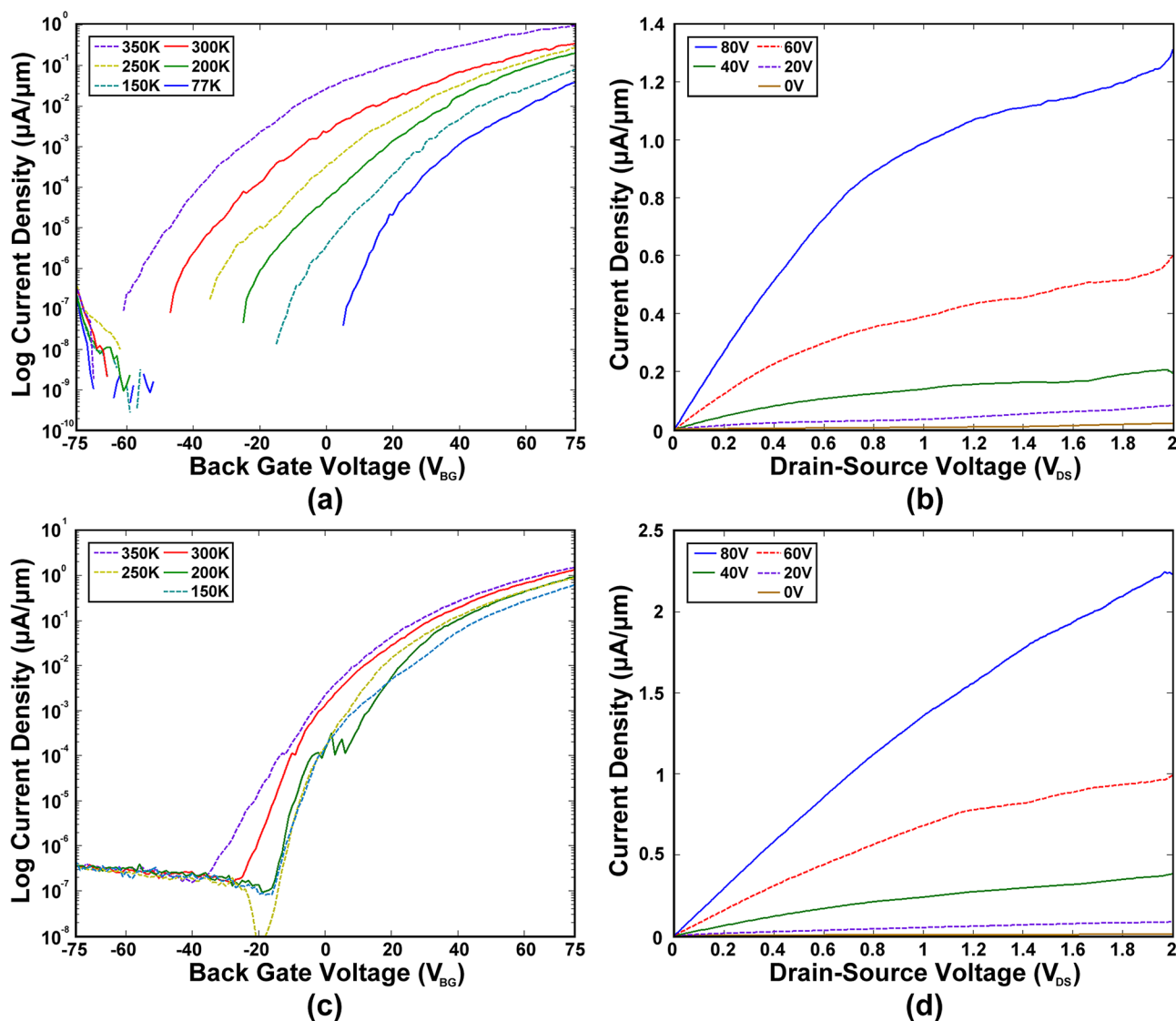


FIG. 2.  $I_{DS}$ - $V_{GS}$  characteristics taken at  $V_{DS} = 1$  V for various temperatures (a), (c) and  $I_{DS}$ - $V_{DS}$  characteristics at 300 K (b), (d) for the same  $L/W = 400$  nm/1000 nm transistor before (a), (b) and after (c), (d) the deposition of a 15 nm ALD  $Al_2O_3$  overcoat.

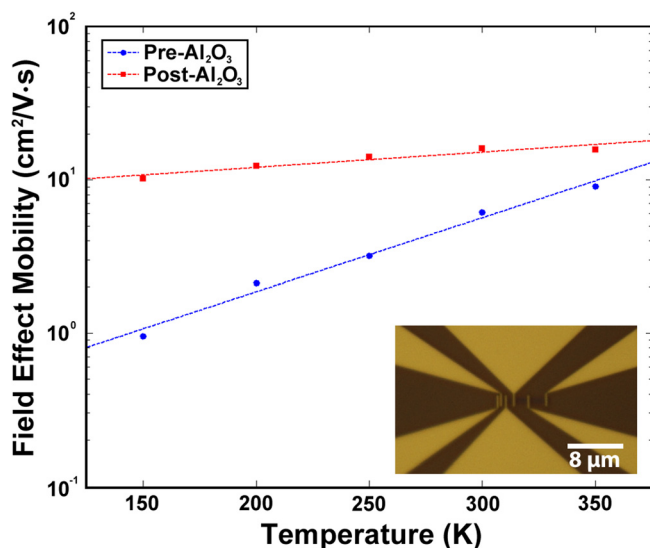


FIG. 3. Field effect mobility measured for the same  $L/W = 800$  nm/1000 nm at  $V_{DS} = 0.5$  V before and after the deposition of a 15 nm ALD  $Al_2O_3$  overcoat; the inset shows an optical micrograph of our finished device.

an indirectly improved mobility.<sup>19</sup> We observed that while our devices were intrinsically n-doped as a result of processing (a negative bias voltage required to reach complete channel pinch-off), the temperature dependence of the threshold voltage was significantly reduced after the  $Al_2O_3$  growth. Additionally, the on/off ratio was reduced from  $10^9$  to  $10^7$  suggesting that the doping mechanism in the  $MoS_2$  is related to optical phonon scattering.<sup>20</sup>

In conclusion, back-gated, n-channel MOSFETs were fabricated on individual CVD-grown single-layer  $MoS_2$  crystals. The electrical properties of the devices were measured both before and after the deposition of a 15 nm ALD  $Al_2O_3$  overcoat, which was shown to significantly improve the channels on-state conductance and increase the back-gated mobility by a factor of  $\sim 3$  at room temperature, despite the large contact resistance measured for these devices. While measurements indicate a significantly lower FET mobility using strictly a back-gate compared to dual-gated FET devices, we obtained similar performance to devices fabricated from exfoliated material with the addition of a high- $\kappa$  coating enhancing the performance of CVD-grown  $MoS_2$ .

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